IN THE UNITED STAPES PATENT AND TRADEMARK OFFICE

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In re application of: Chen, et al.

Serial No. 10/712460

Filed: November 13, 2003

For: SEMICONDUCTOR WAFER MANUFACTURING METHODS EMPLOYING CLEANING DELAY

PERIOD

Attorney Docket No. 24061.42

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Group Art Unit: Unknown

Examiner: Unknown

LETTER TO THE OFFICIAL DRAFTSPERSON

Attn: Official Draftsperson Commissioner For Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

Enclosed are two (2) sheets of formal drawings to replace the informal drawings as originally filed in the above-identified patent application.

Respectfully submitted,

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File: 24061.42

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on December 22003.

Gayle Conner